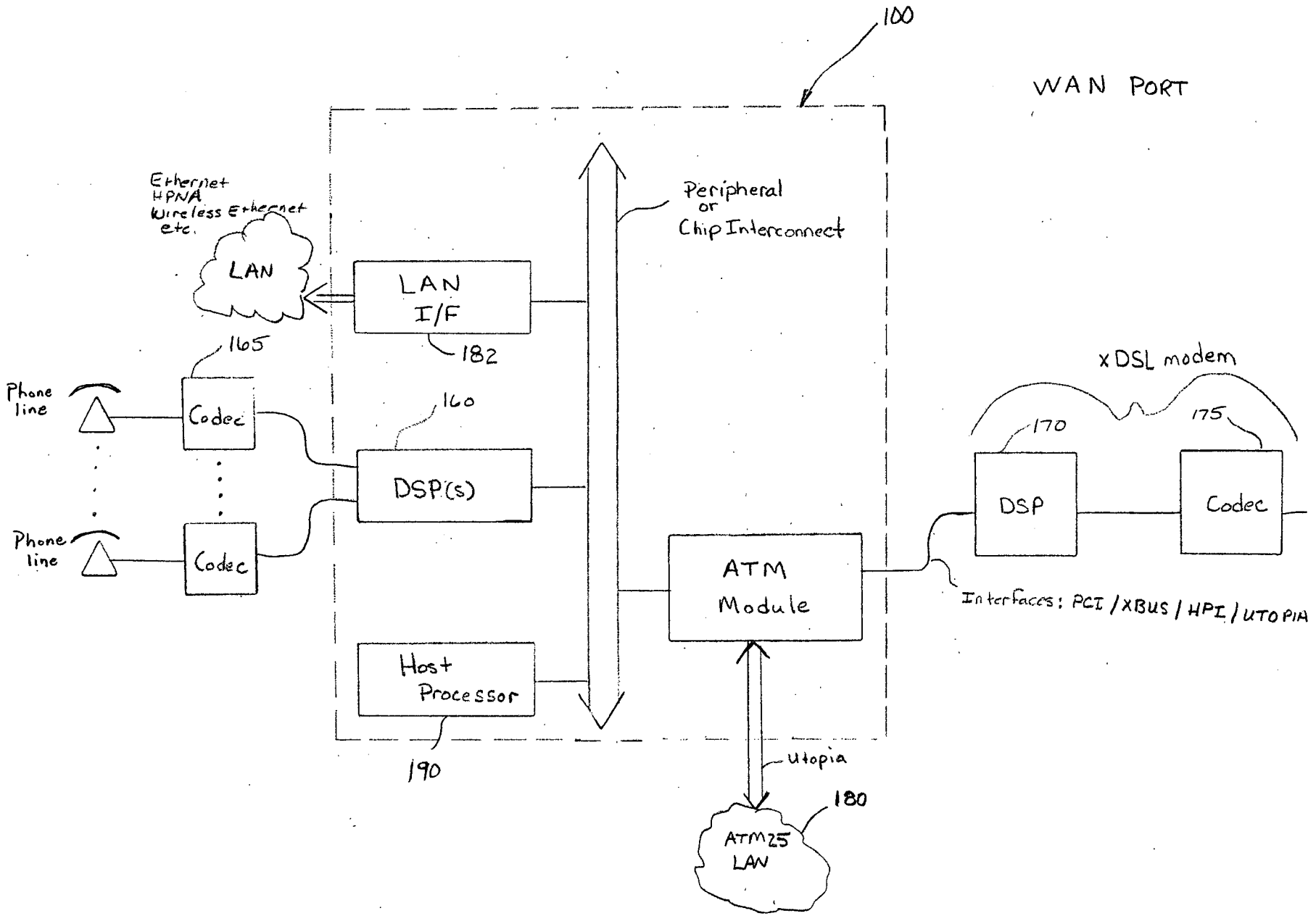
100
WAN PORT
Ethernet
HPNA
Wireless Ethernet
etc.
LAN
LAN I/F
182
Peripheral or Chip Interconnect
165
Phone line
Codec
Phone line
Codec
160
DSP(s)
Host Processor
190
ATM Module
Utopia
180
ATM25 LAN
xDSL modem
170
DSP
175
Codec
Interfaces: PCI / XBUS / HPI / UTOPIA

Figure 1

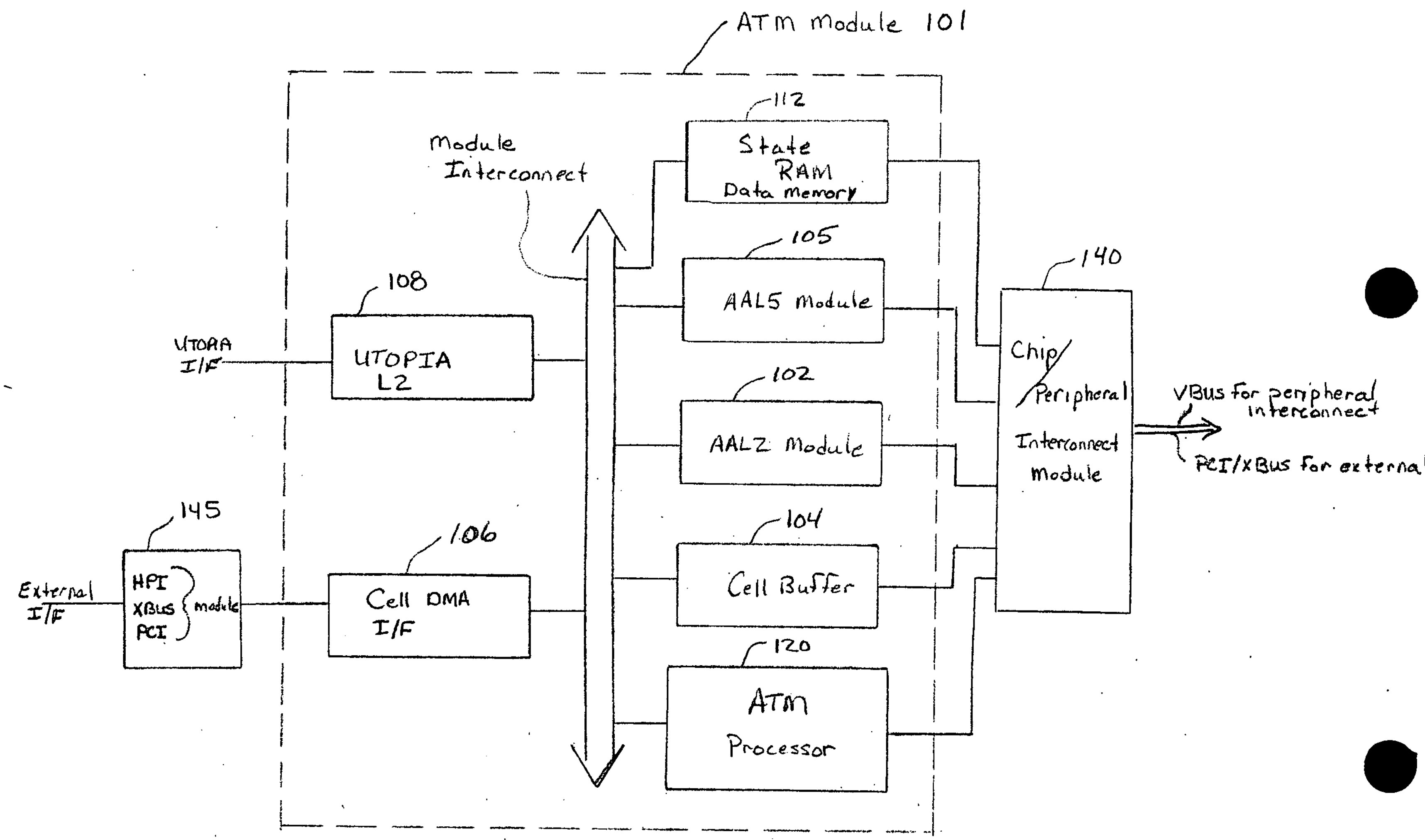
ATM module 101
112
State
RAM
Data memory
Module
Interconnect
105
AAL5 Module
108
UTOPIA
L2
UTOPIA
I/F
102
AAL2 Module
140
Chip/Peripheral
Interconnect
Module
VBus for peripheral interconnect
PCI/XBus for external
145
HPI
XBus
PCI
module
External
I/F
106
Cell DMA
I/F
104
Cell Buffer
120
ATM
Processor

Figure 2

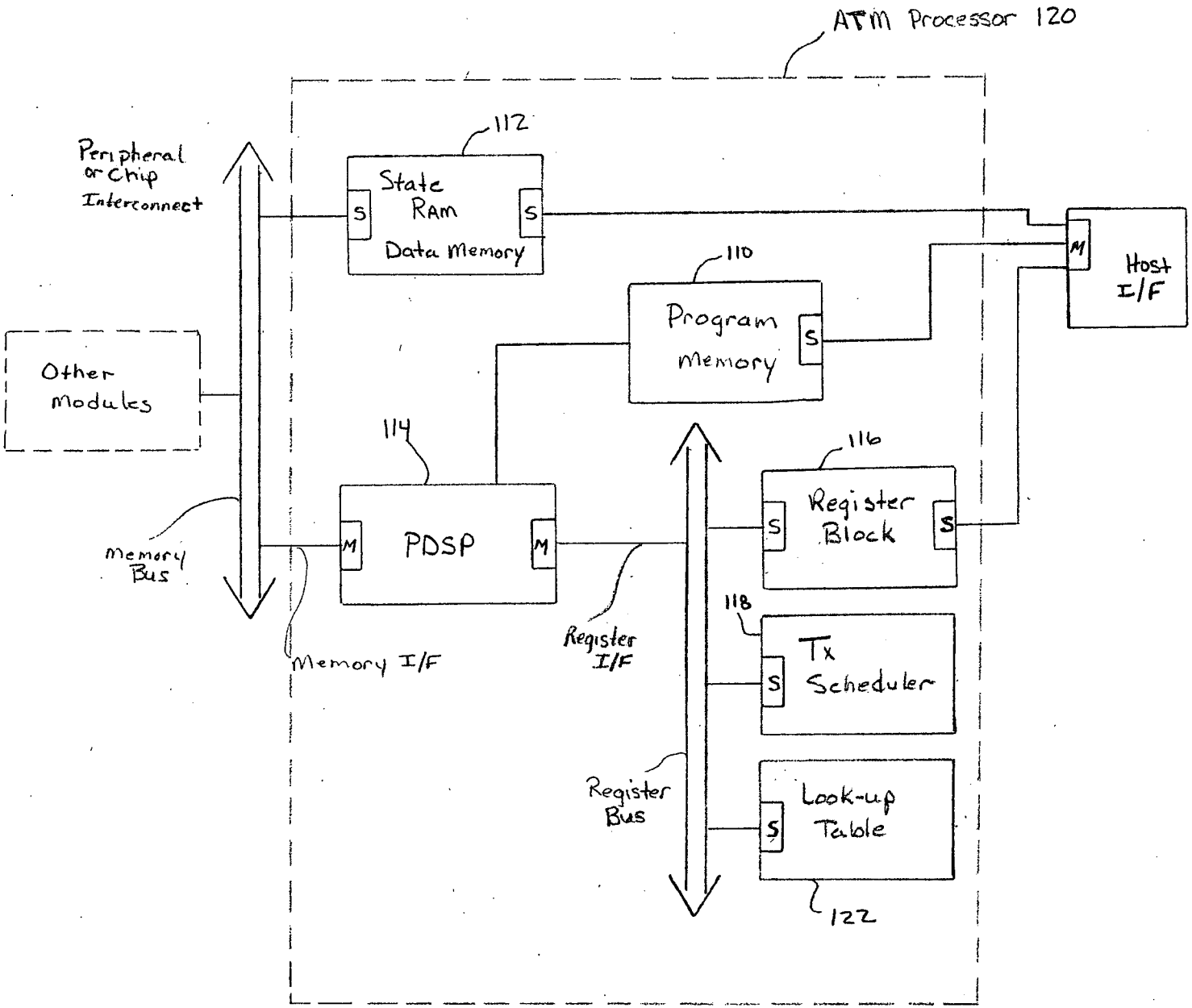
ATM Processor 120
112
State RAM
Data Memory
S
S
Peripheral or Chip Interconnect
110
Program Memory
S
M
Host I/F
Other Modules
114
PDSP
M
M
Memory Bus
Memory I/F
Register I/F
116
Register Block
S
S
118
Tx Scheduler
S
Register Bus
Look-up Table
S
122

Figure 3

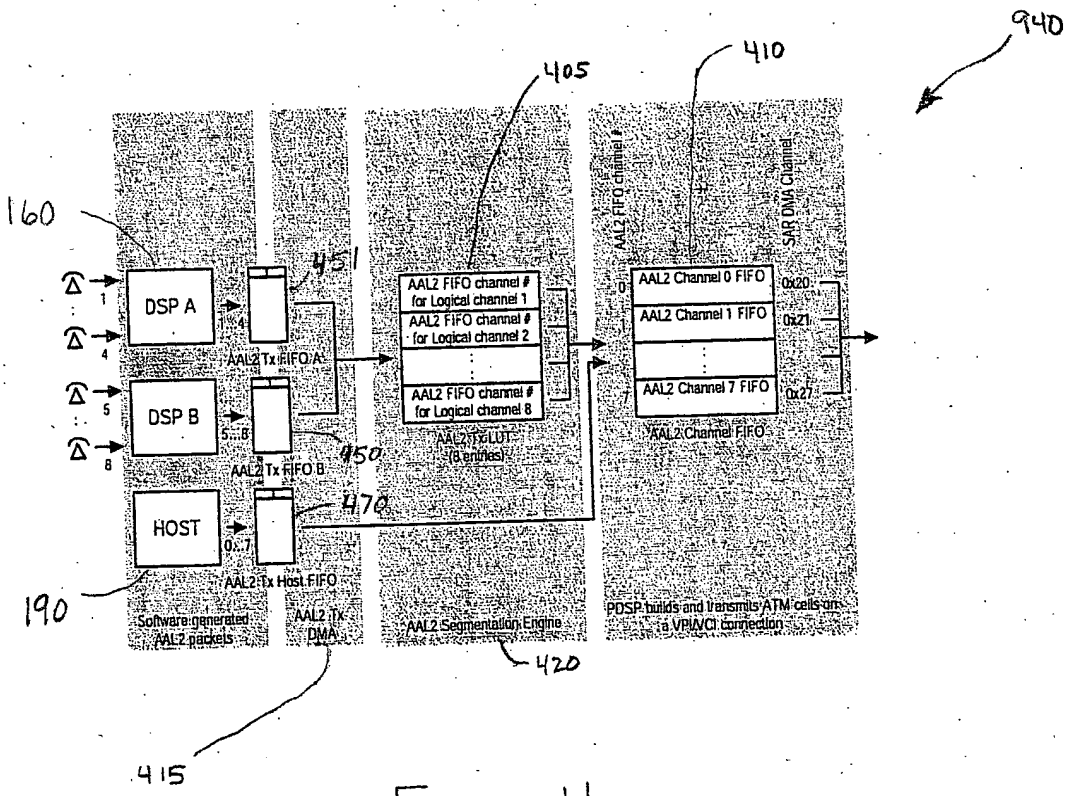
940
410
405
160
451
DSP A
DSP B
HOST
AAL2 Tx FIFO A
AAL2 Tx FIFO B
AAL2 Tx Host FIFO
450
470
190
415
AAL2 FIFO channel # for Logical channel 1
AAL2 FIFO channel # for Logical channel 2
AAL2 FIFO channel # for Logical channel 8
AAL2 Tx LUT (8 entries)
AAL2 FIFO channel #
SAR DMA Channel
AAL2 Channel 0 FIFO
AAL2 Channel 1 FIFO
AAL2 Channel 7 FIFO
0x20
0x21
0x27
AAL2 Channel FIFO
Software generated AAL2 packets
AAL2 Tx DMA
AAL2 Segmentation Engine
420
PDSP builds and transmits ATM cells on a VPI/VCI connection

Figure 4

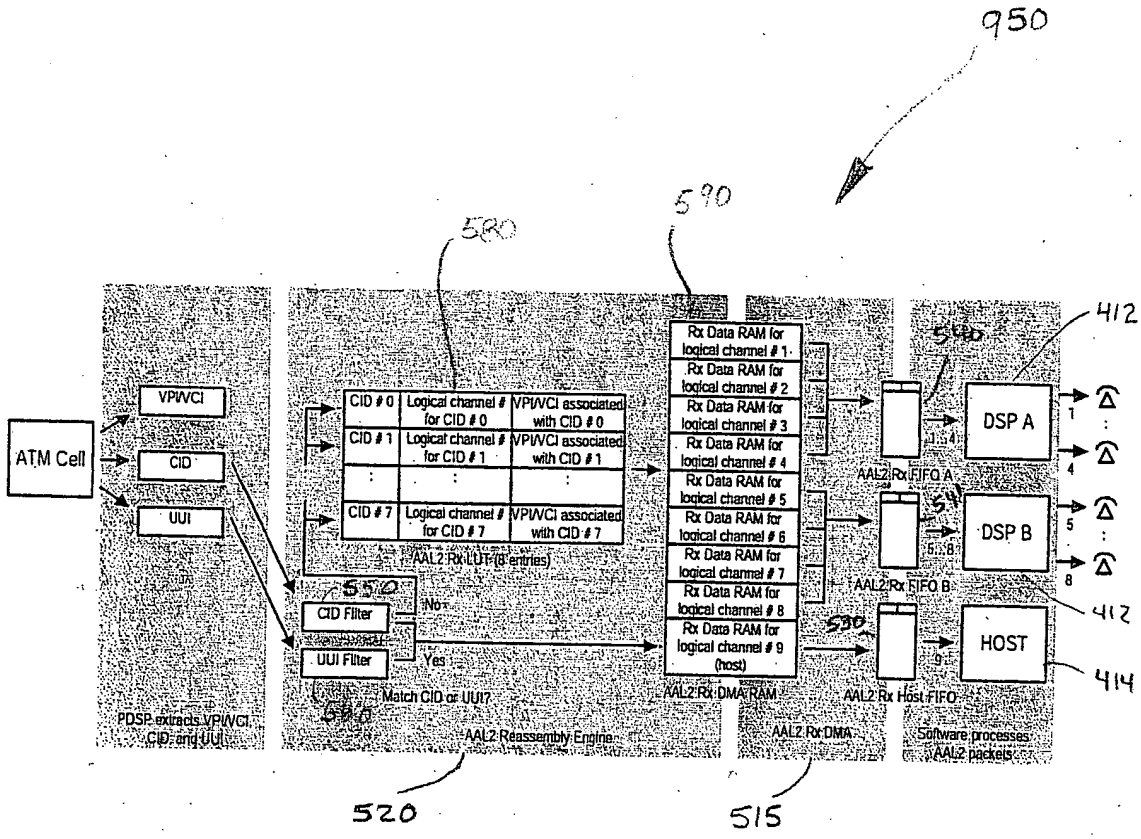
950
580
590
412
540
ATM Cell
VPI/VCI
CID
UUI
CID # 0
Logical channel # for CID # 0
VPI/VCI associated with CID # 0
CID # 1
Logical channel # for CID # 1
VPI/VCI associated with CID # 1
CID # 7
Logical channel # for CID # 7
VPI/VCI associated with CID # 7
AAL2 Rx LUT (8 entries)
550
CID Filter
No
UUI Filter
Yes
Match CID or UUI?
560
PDSP extracts VPI/VCI, CID and UUI
AAL2 Reassembly Engine
520
Rx Data RAM for logical channel # 1
Rx Data RAM for logical channel # 2
Rx Data RAM for logical channel # 3
Rx Data RAM for logical channel # 4
Rx Data RAM for logical channel # 5
Rx Data RAM for logical channel # 6
Rx Data RAM for logical channel # 7
Rx Data RAM for logical channel # 8
Rx Data RAM for logical channel # 9 (host)
AAL2 Rx DMA RAM
AAL2 Rx DMA
515
AAL2 Rx FIFO A
AAL2 Rx FIFO B
AAL2 Rx Host FIFO
530
DSP A
DSP B
HOST
1
4
5
8
9
412
414
Software processes AAL2 packets

Figure 5

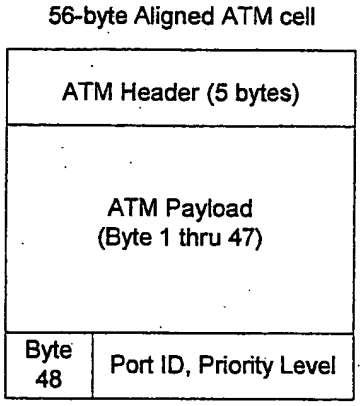

Figure 7

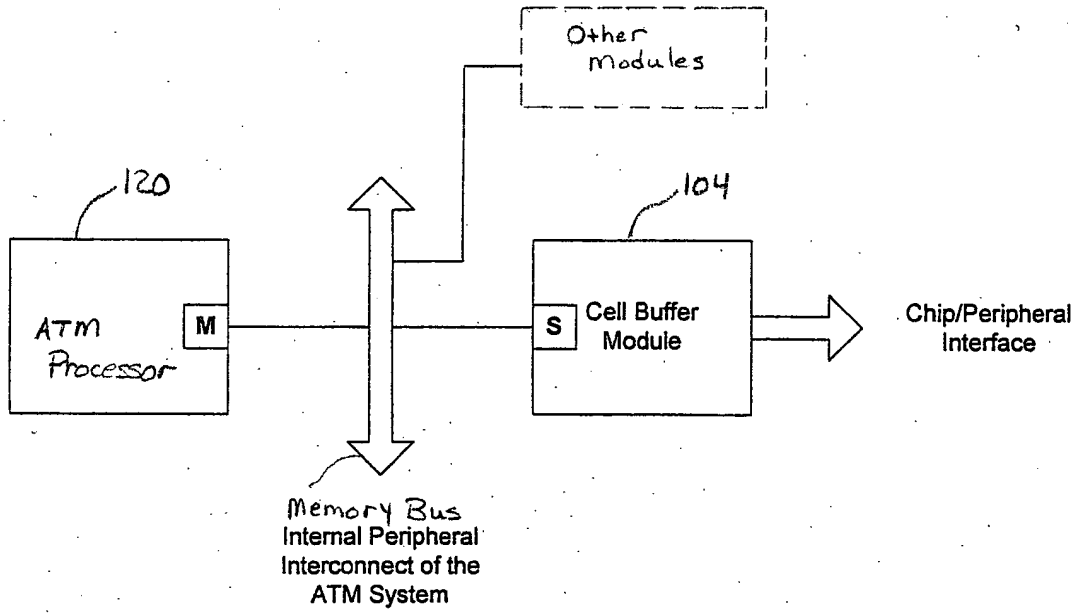

Figure 6A

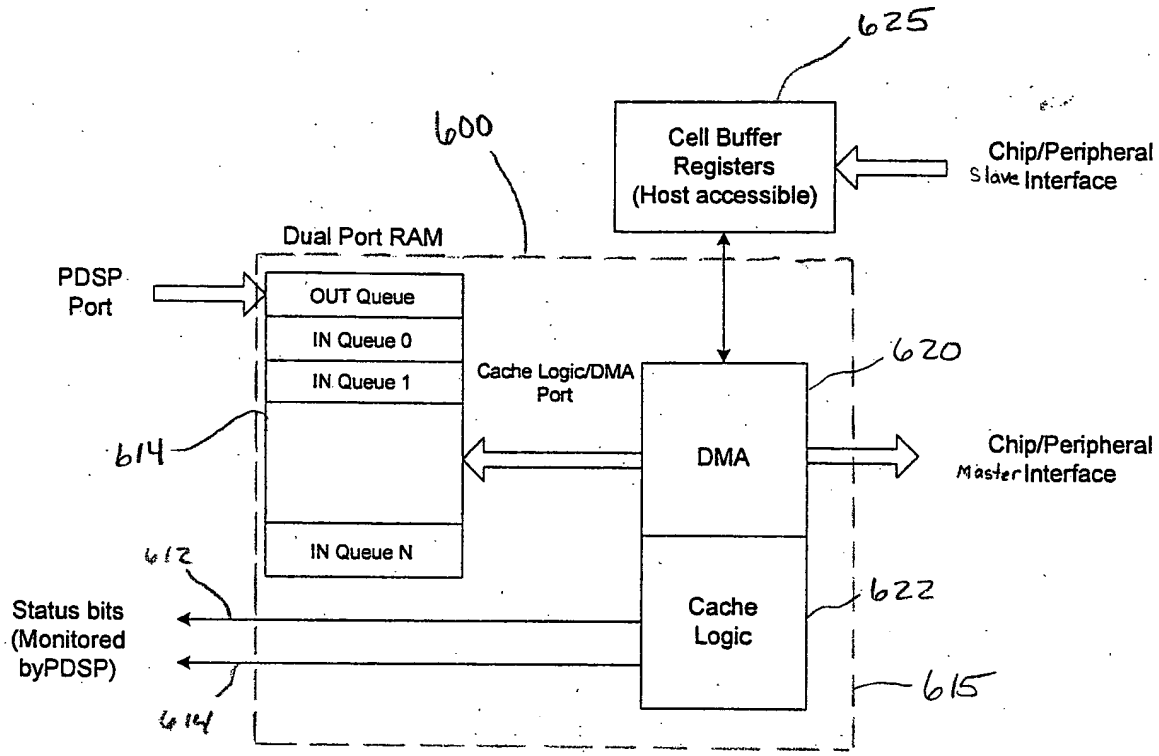
625
600
Cell Buffer Registers (Host accessible)
Chip/Peripheral Slave Interface
Dual Port RAM
PDSP Port
OUT Queue
IN Queue 0
IN Queue 1
IN Queue N
614
Cache Logic/DMA Port
620
DMA
Chip/Peripheral Master Interface
612
Status bits (Monitored byPDSP)
622
Cache Logic
615
614

Figure 6B

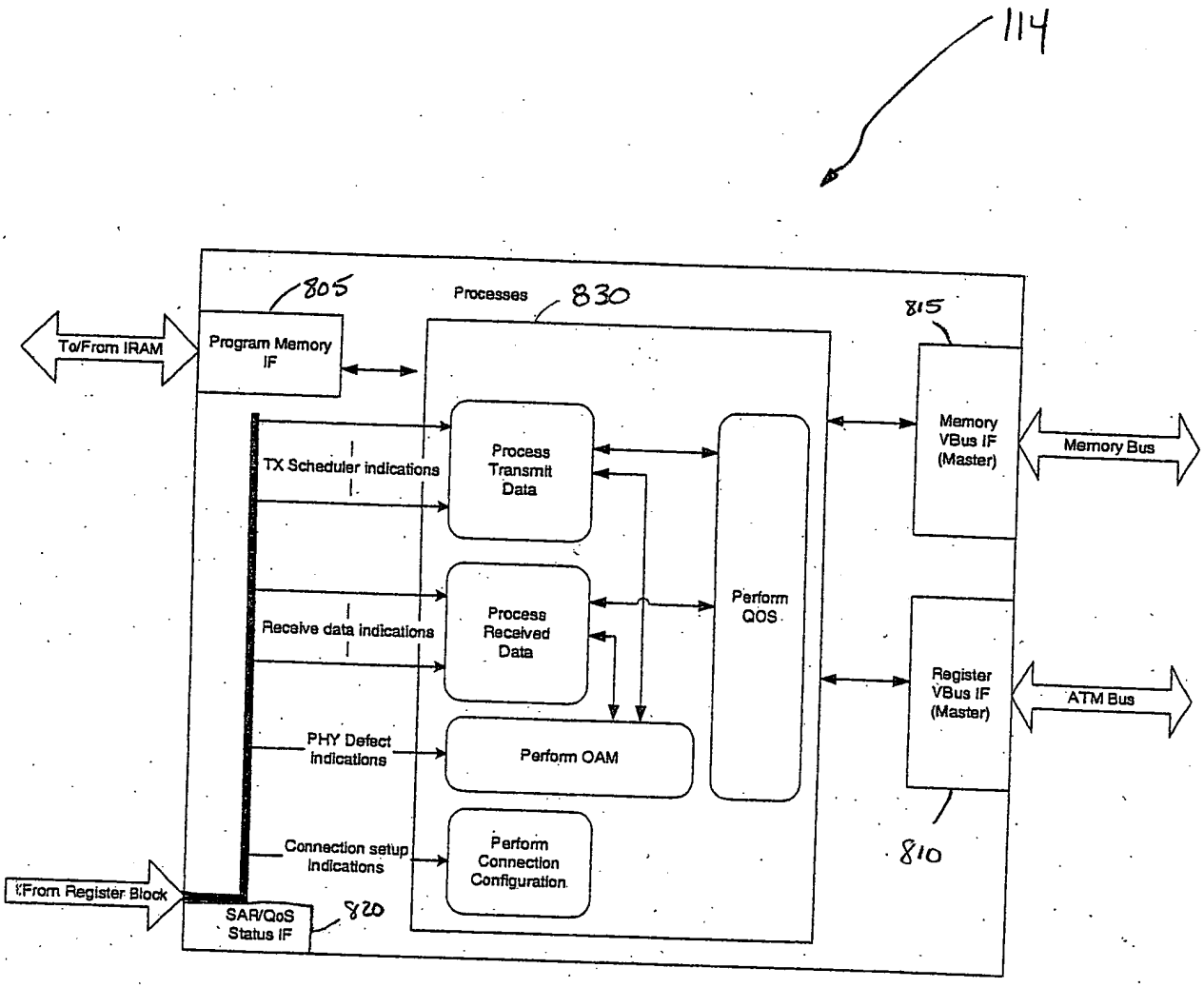
114
805
Processes
830
815
To/From IRAM
Program Memory IF
TX Scheduler indications
Process Transmit Data
Memory VBus IF (Master)
Memory Bus
Receive data indications
Process Received Data
Perform QOS
PHY Defect indications
Perform OAM
Register VBus IF (Master)
ATM Bus
Connection setup indications
Perform Connection Configuration
810
From Register Block
SAR/QoS Status IF
820

Figure 8